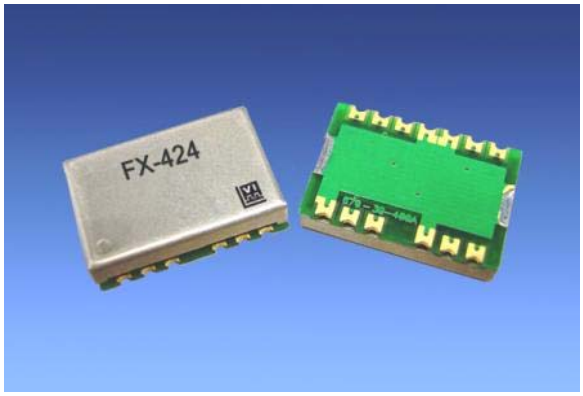
FX-424
Low Jitter Frequency Translator



Features

- **Quartz-based PLL for Ultra-Low Jitter**
- **Frequency Translation up to 850 MHz**
- **Accepts up to 4 ext.-muxed clock inputs**
- **CMOS / LVDS / LVPECL Inputs compatible**
- **Differential LVPECL / LVDS or LVCMOS Output**
- **Lock Detect / Loss of Signal Alarms**
- **Output Disable**
- **20.3 x 13.7 x 5.1 mm SMT package**
- **RoHS/Lead Free Compliant**

Description

The FX-424 is a precision quartz-based frequency translator used to translate an input frequency such as 8 kHz, 1.544 MHz, 2.048 MHz, 19.44 MHz etc. to any specific frequency from 1.544 MHz to 850 MHz. The FX-424 can perform either up or down frequency conversion. The FX-424's superior jitter performance is achieved through the use of a precision VCXO or VCSO. With the use of an external multiplexer, up to 4 different input clocks can be translated to a common output frequency.

Applications

- **Wireless Infrastructure**
- **10 Gigabit FC**
- **Synchronous Ethernet**
- **OADM and IP Routers**
- **Test Equipment**
- **Military Communications**

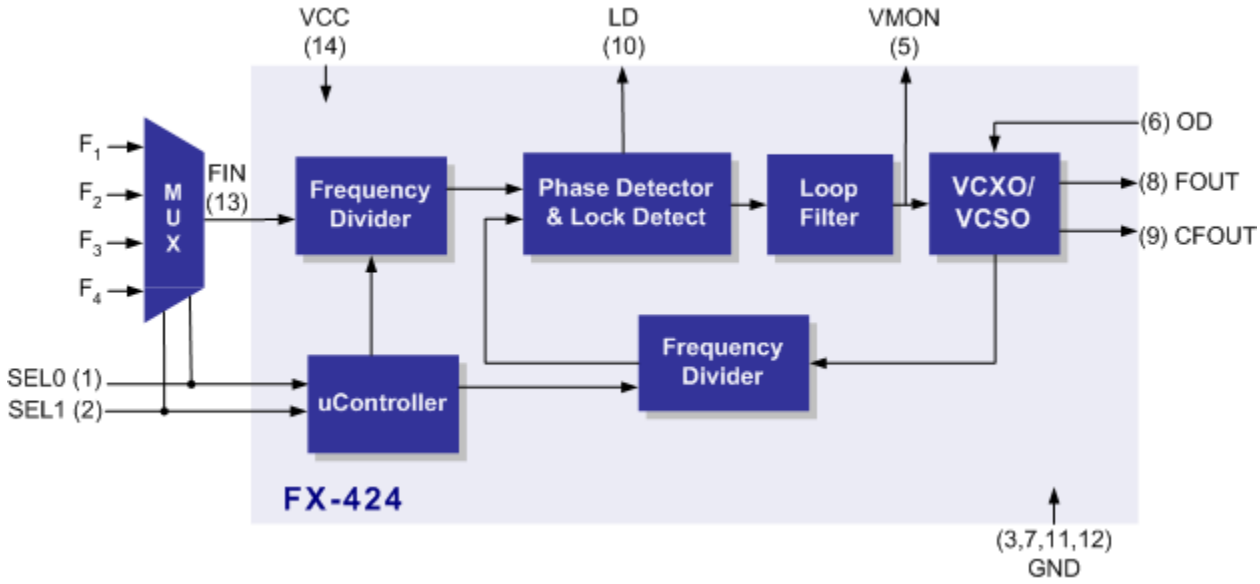


Figure 1. Functional Block Diagram

Table 1. Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Input Frequency	F_{IN}	0.008		170	MHz	1,2,3
Capture Range	APR	±40			ppm	1,2,3
Output Frequency	F_{OUT}	1.544		850	MHz	1,2,3
Supply						
Voltage	V_{CC}	3.13	3.3	3.46	V	2,3
Current (No Load)	I_{CC}		45	60	mA	3
Input Signal						
CMOS	F_{IN}		CMOS			2,3
LVPECL	F_{IN}		LVPECL			
LVCMOS Output (Option A)			LVCMOS			2,3
Differential Output (Options F and P)						
Mid Level - LVPECL		V_{CC}-1.4	V_{CC}-1.25	V_{CC}-1.0	V	2,3
Swing - LVPECL		450	600	950	mV-pp	2,3
Mid Level - LVDS		V_{CC}-2.4	V_{CC}-2.3	V_{CC}-2.5	V	2,3
Swing - LVDS		250	410	450	mV-pp	2,3
Rise Time	t_R		0.5		ns	4,5
Fall Time	t_F		0.5		ns	4,5
Symmetry	SYM	45	50	55	%	2,3
SSB Phase Noise, F_{OUT} **=** 155.52/622.08						
@ 10 Hz Offset	Φ_n		-64/-27		dBc/Hz	5,6
@ 100 Hz Offset	Φ_n		-95/-55		dBc/Hz	
@ 1 kHz Offset	Φ_n		-123/-85		dBc/Hz	
@ 10 kHz Offset	Φ_n		-143/-110		dBc/Hz	
@ 100 kHz Offset	Φ_n		-146/-130		dBc/Hz	
@ 1 MHz Offset	Φ_n		-146/-146		dBc/Hz	
@ 10 MHz Offset	Φ_n		-146/-146		dBc/Hz	
Jitter Generation						
155.52 MHz (12 kHz – 20 MHz BW)	Φ_J		0.30		ps RMS	5, 6
622.08 MHz (12 kHz – 20 MHz BW)	Φ_J		0.12		ps RMS	
Operating Temperature	T_{OP}	-40		85	°C	1,3

1. See Standard Frequencies and Ordering Information.
2. Parameters are tested with production test circuit below (Fig 2).
3. Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
4. Measured from 20% to 80% of a full output swing (Fig 3).
5. Not tested in production, guaranteed by design, verified at qualification.
6. The FX-424 phase noise and jitter performance can be optimized for specific applications. Please consult with Vectron's Application Engineers for more information.

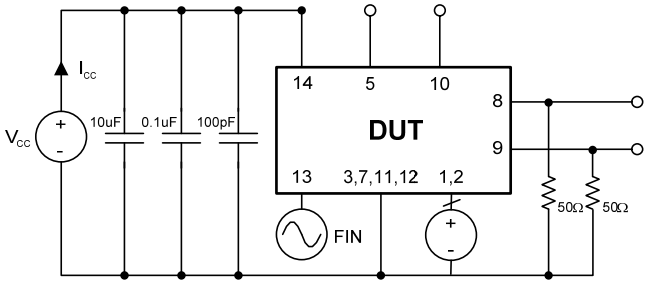


Figure 2. Test Circuit

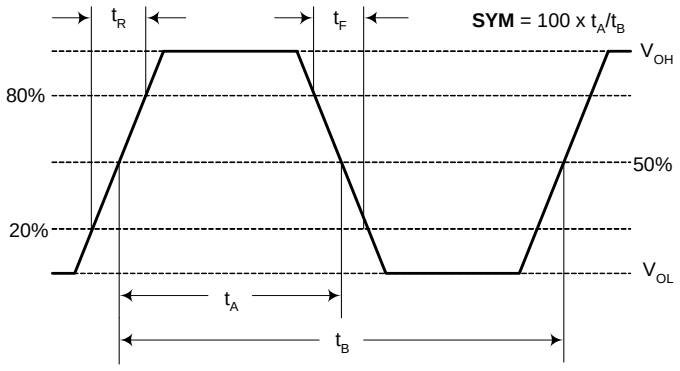


Figure 3. LVPECL Waveform

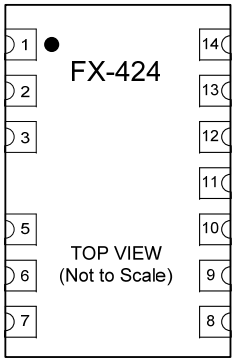


Figure 4. Pin Configuration

Table 2. Pin Out

Pin #	Symbol	I/O	Level	Function
1	SEL0	I	LVTTL	Input Frequency Select*
2	SEL1	I	LVTTL	Input Frequency Select*
3	GND	GND	Supply	Case and Electrical Ground
4				Not present
5	VMON	O	Analog	VCXO Control Voltage Monitor Under locked conditions VMON should be > 0.3V and <3.0V. The input frequency may be out of range if the voltage exceeds these levels.
6	OD	I	LVCMOS	Output Disable Disabled = Logic “1” Enabled = Logic “0” or no connect
7	GND	GND	Supply	Case and Electrical Ground
8	FOUT	O	LVPECL, LVDS, or LVCMOS	Frequency Output
9	CFOUT	O or GND	LVPECL, LVDS, or LVCMOS	Complementary Frequency Output – Note for LVCMOS option this pad will be tied to GND.
10	LD	O	LVCMOS	Lock Detect Locked = Logic “1” Loss of Signal = Logic “0”
11	GND	GND	Supply	Case and Electrical Ground
12	GND	GND	Supply	Case and Electrical Ground
13	FIN	I	LVCMOS or LVPECL	Input Frequency. The FX-424 series AC couples the input for handling of either LVCMOS or LVPECL input signals.
14	VCC	VCC	Supply	Power Supply Voltage (3.3 V ±5%)

* For applications requiring two to four input frequencies, Vectron will assign a unique part number and the Input Frequency versus SEL[1:0] settings will be provided in a Specification Control Drawing. For single input configurations it is recommended that SEL0 and SEL1 are tied to ground.

Outline Diagram

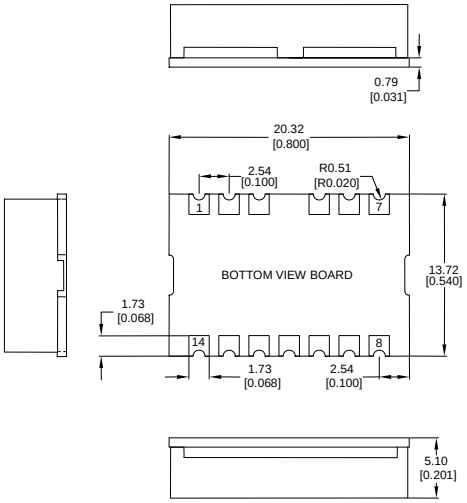


Figure 5.

Suggested Pad Layout

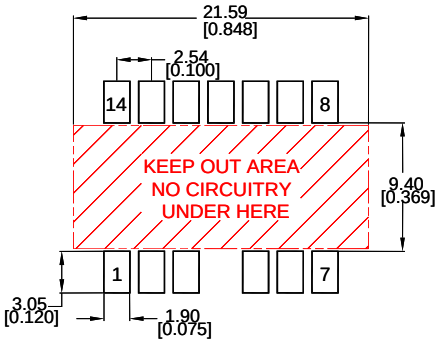


Figure 6.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Output Current	I_{OUT}		mA
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260/40	°C/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The FX-424 family is undergoing the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the FX-424 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation

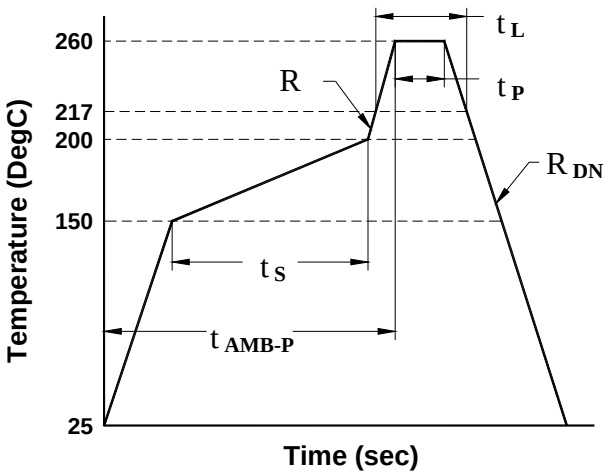
ESD Ratings

Model	Minimum	Conditions
Human Body Model	500 V	MIL-STD 883, Method 3015
Charged Device Model	500 V	JEDEC, JESD22-C101

Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The FX-424 is being qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-424 should not be subjected to a wash process that will immerse it in solvents. NO CLEAN is the recommended procedure. The FX-424 has been designed for pick and place reflow soldering. The FX-424 may be reflowed once and should not be reflowed in the inverted position.



Application Circuits

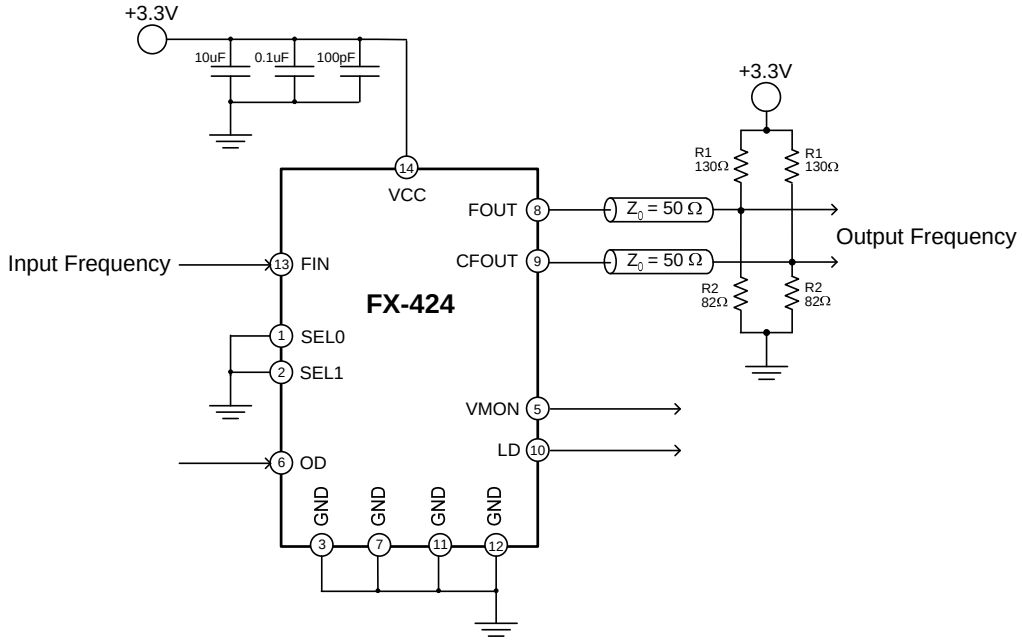


Figure 7. Single Input Frequency Translation - LVPECL Termination

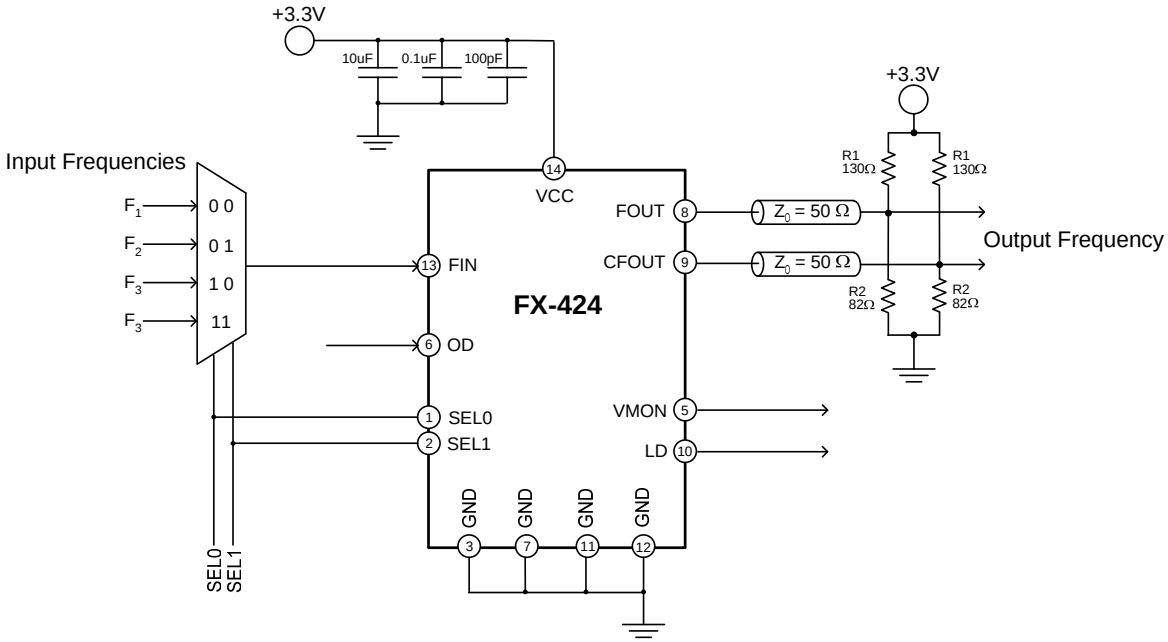
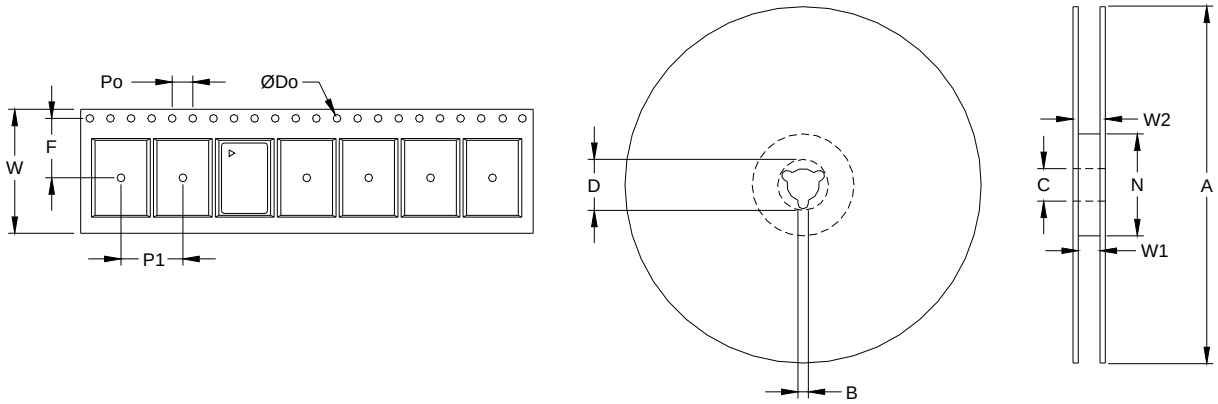


Figure 8. Four Input Frequencies Translated to Common Output Frequency – LVPECL Termination

Tape and Reel (EIA-481-2-A)



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**# Per**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Min**	**Typ**	**Min**	**Min**	**Typ**	**Max**	**Reel**
FX-424	44	20.2	1.5	4	20	330	1.5	13	20.2	100	44.4	50.4	100

Vectron plans to offer both tape-n-reel and matrix trays as packaging options for the FX-424. The standard shipping container for volume production is a matrix tray. The trays are 100% recyclable and offer the added feature that they can be continuously fed into a pick-n-place machine. (Matrix tray drawing not currently available)

Standard Frequencies

8 kHz	**C**	26.00 MHz	**T**	622.08 MHz	**8**
16 kHz	**D**	27.00 MHz	**W**	666.5143 MHz	**9**
64 kHz	**E**	38.88 MHz	**X**		
1.024 MHz	**F**	44.736 MHz	**Y**		
1.544 MHz	**H**	51.84 MHz	**0**		
2.048 MHz	**J**	61.44 MHz	**1**		
4.096 MHz	**K**	77.76 MHz	**2**		
8.192 MHz	**L**	82.944 MHz	**3**		
13.000 MHz	**M**	112.000 MHz	**4**		
16.384 MHz	**N**	139.264 MHz	**5**		
19.440 MHz	**P**	155.520 MHz	**6**		
20.480 MHz	**R**	166.6286 MHz	**7**	Special SCD	**S**

Not all combinations are possible.

Ordering Information

FX-424 - X X X - X X X X X

Product Family
FX: Frequency Translator

Package
424: 20.3 x 13.0 x 5.1 mm

Supply Voltage
D: 3.3 Vdc ± 5%

Output Type
A: LVCMOS
F: LVPECL (Complementary)
P: LVDS (Complementary)

Operating Temperature
C: 0 to 70°C
F: -40 to 85°C

Input Logic
A: LVCMOS
D: LVPECL

Number of Input Frequencies
1: 1 input frequency
2: 2 input frequencies[2]
3: 3 input freuqencies[2]
4: 4 input frequencies[2]

Input Frequency
See Above.[1,2]

Output Frequency
See Above[1].

RoHS Compliant
G: Yes
Blank: May contain Pb

1. For non-listed frequencies and/or multiple input frequencies a unique part number will be assigned with the following format FX-424-XXX-SNNNN. "SNNNN" is the SCD number.
2. To request *initial samples* for an FX-424 with more than one input frequency, please use the following format FX-424-XXX-XNSX followed by the input frequencies. For example, to request samples for a translator with and operating temperature of -40 to +85°C, input frequencies of 8 kHz, 1.544 MHz, 19.44 MHz, 77.76 MHz and an output frequency of 622.08 MHz, the part number would be FX-424-DFF-A4S8, S = 8 kHz, 1.544 MHz, 19.44 MHz, 77.76 MHz.

For Additional Information, Please Contact:

VECTRON INTERNATIONAL A DOVER COMPANY

USA: Vectron International, 267 Lowell Rd, Hudson, NH 03051 . . . . **Tel: 1-88-VECTRON-1** **Fax: 1-888-FAX-VECTRON**
EUROPE: . . . . **Tel: +49 (0) 7268 8010** **Fax: +49 (0) 7268 8012 81**
ASIA: . . . . **Tel: +86-21-5048-0777** **Fax: +86-21-5048-1881**

Revision History:

Revision	Date	Salesman Approval	Eng req'd	Engineer Approval	Date	Description
A	10/02/06	BW				Added LVDS option to Ordering Information. Table 1 updated. Pad layout drawing modified.
1	12/08/06	BW				Official Release. Outline diagram updated.
1.1	12/20/07	BW				Added LVDS output option to ordering information.